ABSTRACT OF THE DISCLOSURE

A semiconductor memory device comprises a substrate; a first semiconductor layer of a first conduction type having a single crystalline structure isolated from the substrate by an insulator layer; a plurality of memory transistors, each having a gate electrode connected to a word line, a pair of impurity regions of a second conduction type serving as a drain region and a source region formed in the first semiconductor layer, and a channel body of the first conduction type formed in the first semiconductor layer between the impurity regions, and operative to store data as a state of majority carriers accumulated in the channel body; a plurality of device isolation regions formed to isolate memory transistors having gate electrodes commonly connected to the same word line from each other among the plurality of memory transistors; and a plurality of impurity region isolation regions formed to isolate adjacent drain regions from each other and adjacent source regions from each other, the impurity region isolation region having a smaller width than that of the device isolation region.